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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/813,433	03/31/2004	Simon Knowles	321546US	3801

27964 7590 01/11/2011

HITT GAINES P.C.
P.O. BOX 832570
RICHARDSON, TX 75083

EXAMINER	
HUISMAN, DAVID J	

ART UNIT	PAPER NUMBER
2183	

NOTIFICATION DATE	DELIVERY MODE
01/11/2011	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

docket@hittgaines.com

Office Action Summary	Application No.	Applicant(s)	
	10/813,433	KNOWLES, SIMON	
	Examiner	Art Unit	
	DAVID J. HUISMAN	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 November 2010*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10,12,13,15-22 and 30-32* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10,12,13,15-22 and 30-32* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *31 March 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *11/24/2010*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date: _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-10, 12-13, 15-22, and 30-32 have been examined.

Information Disclosure Statement

2. The document cited in the IDS submitted on November 24, 2010, has not been considered (denoted by strike-through) because applicant is required, per 37 CFR 1.98(a)(3)(i), to provide "A concise explanation of the relevance, as it is presently understood by the individual designated in § 1.56(c) most knowledgeable about the content of the information, of each patent, publication, or other information listed that is not in the English language. The concise explanation may be either separate from applicant's specification or incorporated therein." Since an English copy of the cited NPL document was not provided, and applicant also did not provide the concise statement required by 37 CFR 1.98, this document has not been considered.

Drawings

3. The drawings are objected to because the text is too small. 37 CFR 1.87(p)(3) requires that all numbers, letters, and reference characters measure at least 1/8 inches in height. The examiner asserts that the majority of the text does not satisfy this requirement. Recall from 37 CFR 1.87(k) that drawings are reduced in size to two-thirds in reproduction. Hence, such small text will be difficult to read if not increased in size. Please locate the small text and enlarge it.

4. The drawings are objected to because they do not comply with 37 CFR 1.84(u), which requires that view numbers must be preceded by the abbreviation "FIG.". Therefore, application should replace "FIGURE" in each of the drawings with --FIG.--.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Objections

5. Claim 1 is objected to because of the following informalities:

- In the 2nd to last line on page 2, replace "the operand" with --the at least one operand--.
- On page 3, line 1, replace "a" with --said--.

6. Claim 22 is objected to because of the following informalities:

- On page 7, line 3, replace "the operand" with --the at least one operand--.

7. Claim 30 is objected to because of the following informalities:

- On page 8, 6th to last line, replace "the operand" with --the at least one operand--.
- On page 8, 4th to last line, replace "a" with --said--.

8. Claim 31 is objected to because of the following informalities:

- On page 10, line 2, replace "the operand" with --the at least one operand--.
- On page 10, line 4, replace "a" with --said--.

9. Claim 32 is objected to because of the following informalities:

- On page 11, line 7, should "prove" be replaced with --provide--?
- On page 11, 9th to last line, replace "the operand" with --the at least one operand--.
- On page 11, 7th to last line, replace "a" with --said--.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

10. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

11. Claims 12-13 and 16 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

12. Claim 12 recites the limitation "the configurable operators" in the last line. There is insufficient antecedent basis for this limitation in the claim because it is not clear if applicant is referring to the configurable operators of claim 12, line 2, the configurable operators of claim 9, line 1, or the configurable operators recited in claim 1.

13. Claim 13 recites the limitation "said configurable operators" in the last line. There is insufficient antecedent basis for this limitation in the claim because it is not clear if applicant is referring to the configurable operators of claim 12, line 2, the configurable operators of claim 12, last line, the configurable operators of claim 9, line 1, or the configurable operators recited in claim 1.

14. Claim 16 recites the limitation "said operands" in line 2. There is insufficient antecedent basis for this limitation in the claim because applicant sets forth at least one operand in claim 1. Therefore, where there is just one operand, there is no basis for "said operands".

Double Patenting

15. Applicant is advised that should claims 30-32 be found allowable, claims 16, 5, and 12 will be objected to under 37 CFR 1.75 as being substantial duplicates of claims 30-32, respectively. When two claims in an application are duplicates or else are so close in content that they both cover the same thing, despite a slight difference in wording, it is proper after allowing one claim to object to the other as being a substantial duplicate of the allowed claim. See MPEP § 706.03(k).

Claim Rejections - 35 USC § 103

16. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

17. Claims 1-10, 12-13, 15-22, and 30-32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Trimberger, U.S. Patent No. 5,737,631, in view of one or more of Haynes et al., "Configurable Multiplier Blocks for use within an FPGA", 1998 (herein referred to as Haynes), Lodi et al., "A Flexible LUT-Based Carry Chain for FPGAs", 2003 (herein referred to as Lodi), and Madurawe, U.S. Patent No. 7,176,713, and further in view of Jacob et al., "Memory Interfacing and Instruction Specification for Reconfigurable Processors", 1999, pp.145-154 (herein referred to as Jacob).

18. Referring to claim 1, Trimberger has taught a hardware computer processor having control and data processing capabilities comprising:

a) a hardware decode unit for decoding instructions and operable to separate control instructions from data processing instructions (Trimberger: Figure 2, item 112). Control instructions for execution unit 100 and data processing instructions for FPGA 120 are inherently separated because the purpose of the decoder is to identify the type of instruction and control the appropriate circuitry to carry out the operation indicated by the instruction. Therefore, if a control instruction exists, appropriate control signals would be sent to unit 100. If a data processing instruction exists, appropriate control signals would be sent to FPGA 120.

b) a dedicated hardware control processing facility comprising a control execution path dedicated to processing said control instructions having its own control register file (Fig.2, component 103 or 140, for instance) and a hardware execution unit (Fig.2, component 100). Note that at least these components may be combined and called a dedicated control processing facility.

c) a dedicated hardware data processing facility (Fig.2, at least component 120) dedicated to processing said data processing instructions, separate from said dedicated control processing

facility, having its own data register file (Fig.2, at least component 130) separate from said control register file, the data processing facility comprising a controller (controllers inherently exist in processors).

d) Trimberger has not taught that the data processing facility comprises a first data execution path including fixed operators and a second data execution path including at least configurable operators, both of said first and second data execution paths separate from said control execution path and each other, said configurable operators pre-configured into a plurality of hardwired operator classes. However, Haynes, Lodi, and Madurawe have taught that FPGAs may be designed to include dedicated circuitry in addition to reconfigurable circuitry. Specifically, Haynes has taught dedicated multiplier blocks, which may be programmably interconnected to create larger multipliers. Similarly, Lodi has taught dedicated carry chains, which may be connected to form, among other things, absolute value and logic function circuitry. See page 133 and sections 3.3 and 4. Madurawe has taught dedicated adders and I/O circuitry in an FPGA for common operations. See column 6, lines 2-4. Essentially, instead of a fully reprogrammable FPGA, as taught by Trimberger, Haynes, Lodi, and Madurawe have taught programmable devices, such as FPGAs, that include fixed and configurable circuitry. Such a configuration, which is common in a Xilinx Virtex FPGA, for instance, allows programmers to achieve balance between programmability and speed for different applications. One of ordinary skill in the art would have recognized that the hardwired operators of Haynes, Lodi, and Madurawe could be implemented in the FPGA of Trimberger. Such a modification would allow Trimberger to achieve increased speed in cases where dedicated circuitry is faster than programmable circuitry. As a result, in order to increase speed for common operations, it would have been obvious to one

of ordinary skill in the art at the time of the invention to modify Trimberger's gate array such that the data processing facility (Trimberger, Fig.2, at least component 120) comprises a first data execution path including fixed operators (for instance, a fixed adder and I/O path, as taught by Madurawe) and a second data execution path including at least configurable operators (for instance, a configurable multiplier and carry-chain path, as taught by Haynes and Lodi), both of said first and second data execution paths separate from said control execution path and each other (clearly the FPGA paths are separate from each other and from the control path), said configurable operators pre-configured into a plurality of hardwired operator classes (in the proposed combination, the FPGA of Trimberger, as modified, would include configurable operators pre-configured into hardwired multiplier and carry chain classes).

d) Trimberger, as modified, has further taught that said decode unit is operable to supply a said control instruction to a functional unit in said dedicated control processing facility and operable to detect whether one of said data processing instructions defines a fixed data processing instruction or a configurable data processing instruction, said decode unit causing the computer processor to supply said one of said data processing instructions to said first data execution path for processing when a fixed data processing instruction is detected and to said second data execution path for processing when said configurable data processing instruction is detected. See Fig.2, component 112 and column 7, lines 45-50. The examiner asserts that decoders inherently operation in the claimed fashion. They distinguish all types of instructions from each other, and produce the appropriate control signals 113 to control the appropriate circuitry to perform the desired operation.

e) Trimberger has not taught that the dedicated control processing facility also includes functional units comprising a branch unit (despite hinting at existence of a branch unit with disclosure of condition codes (Fig.2)) and a load/store unit. However, the examiner asserts that such units are very well known in the art and are advantageous for providing basic functionality. Branch units are clearly advantageous because they allow for execution of branch instructions. These are at least useful so that loops may be implemented. Loops allow for repeated execution of a block of code without writing the code repetitively within the program. Hence, code size may be decreased. Load and stores, on the other hand, allow for communication data to/from the register file and memory, thereby expanding the usable memory space. As a result, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify Trimberger such that the dedicated control processing facility includes a branch unit and load/store unit.

f) Trimberger has not taught that said configurable data processing instruction indicates at least one operand to be processed and includes an opcode portion defining the operation to be carried out on the operand, and that said controller is operable to configure the connectivity of said configurable operators in accordance with configuration information provided in the opcode portion of said configurable data processing instruction, wherein said configurable operators are arranged to receive said at least one operand. That is, Trimberger is fairly silent on how the FPGA is reconfigured. However, Jacob has taught than an FPGA instruction including an opcode and operands is one way to reconfigure an FPGA. See section 4.2 and Fig.2. Note the FPGA reconfiguration instruction has an opcode (Fig.2 and Table 1, “FPGA function” field) that defines the operation, and at least one operand to be processed (Fig.2, "Rsource" field). One of

ordinary skill in the art would have recognized how straightforward configuration and operation using this configuration on operands would be using such an instruction. In addition, this instruction allows for the configuration and the operation to be triggered with just a single instruction. This is more efficient than an instruction to configure followed by an instruction to trigger operation using that configuration. When a configuration instruction is decoded and detected, it specifies the configuration the FPGA should take on and also the data that is to be processed by the configuration. As a result, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify Trimberger to include a special configurable data processing instruction that indicates at least one operand to be processed and includes an opcode portion defining the operation to be carried out on the operand, and that said controller is operable to configure the connectivity of said configurable operators in accordance with configuration information provided in the opcode portion of said configurable data processing instruction, wherein said configurable operators are arranged to receive said at least one operand. This is a simple and straightforward way to program the FPGA in Trimberger.

19. Referring to claim 2, Trimberger, as modified, has taught a computer processor according to claim 1, wherein the decode unit is capable of decoding a stream of instruction packets from memory, each packet comprising a plurality of instructions (Trimberger: column 7, lines 51-56).

20. Referring to claim 3, Trimberger, as modified, has taught a computer processor according to claim 1, wherein the decode unit is operable to detect if an instruction packet contains a data processing instruction (Trimberger: column 7, lines 45-50).

21. Referring to claim 4, Trimberger, as modified, has taught a computer processor according to claim 1, wherein the configurable operators are configurable at the level of multi-bit values

(Jacob, Table 1 and Fig.2: Note that the configurable operators are configured at a 4-bit (i.e., multibit) level, the 4 bits being specified in the "FPGA function" field of the FPGA instruction).

22. Referring to claim 5, Trimberger, as modified, has taught a computer processor according to claim 4, wherein the configurable operators are configurable at the level of multi-bit values comprising four or more bits (Jacob, Table 1 and Fig.2: Note that the configurable operators are configured at a 4-bit (i.e., multibit) level, the 4 bits being specified in the "FPGA function" field of the FPGA instruction).

23. Referring to claim 6, Trimberger, as modified, has taught a computer processor according to claim 4. Trimberger, as modified, has not taught that the configurable operators are configurable at the level of words. However, a change in size is not given patentable weight. See In re Rose, 105 USPQ 237 (CCPA 1955). One of ordinary skill in the art would have recognized that an FPGA can be configured to operate on various sizes of data, including the size of a system word, which is known in the art. As a result, it would have been obvious to one of ordinary skill in the art at the time of the invention to further modify Trimberger such that the configurable operators are configurable at the level of words.

24. Referring to claim 7, Trimberger, as modified, has taught a computer processor according to claim 1. Trimberger has not taught that a plurality of the fixed operators of the first data execution path is arranged to perform a plurality of fixed operations in independent lanes according to single instruction multiple data principles. However, Official Notice is taken that SIMD and the related advantages are well known and accepted in the art. Specifically, SIMD allows each execution unit to perform the same instruction on different data in the same cycle, thereby increasing data level parallelism. Higher parallelism will potentially result in higher

throughput as more operations can occur at once. Consequently, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify Trimberger such that a plurality of the fixed operators of the first data execution path (Fig.2, component 100) is arranged to perform a plurality of fixed operations in independent lanes according to single instruction multiple data principles.

25. Referring to claim 8, Trimberger, as modified, has taught a computer processor according to claim 1. Trimberger, as modified, has not taught that a plurality of the configurable operators of the second data execution path is arranged to perform multiple operations in different lanes according to single instruction multiple data principles. However, Official Notice is taken that SIMD and the related advantages are well known and accepted in the art. Specifically, SIMD allows each execution unit to perform the same instruction on different data in the same cycle, thereby increasing data level parallelism. Higher parallelism will potentially result in higher throughput as more operations can occur at once. Consequently, it would have been obvious to one of ordinary skill in the art at the time of the invention to further modify Trimberger such that a plurality of the configurable operators of the second data execution path (Trimberger, Fig.2, component 120) is arranged to perform multiple operations in different lanes according to single instruction multiple data principles.

26. Referring to claim 9, Trimberger, as modified, has taught a computer processor according to claim 1, wherein configurable operators of the second execution path are arranged to receive configuration information which determines the nature of the operations performed (this is inherent in all FPGAs).

27. Referring to claim 10, Trimberger, as modified, has taught a computer processor according to claim 9, wherein configurable operators of the second execution path are arranged to receive configuration information which determines the nature of the operations performed from said opcode portion of the configurable data processing instruction (Jacob, section 4.2 and Fig.2).

28. Referring to claim 12, Trimberger, as modified, has taught a computer processor according to claim 9, comprising a control map associated with configurable operators of the second data execution path, said control map being operable to receive at least one configuration bit from a configurable data processing instruction and to provide configuration information to the configurable operators responsive thereto (See Jacob, Table 1 and Fig.2. Note that, in response to at least one FPGA function field bit, a control map (Reconfiguration Bits Table shown in Table 1) provides configuration information to the configurable operators).

29. Referring to claim 13, Trimberger, as modified, has taught a computer processor according to claim 12, wherein said configuration information controls interconnectivity between two or more of said configurable operators (this is inherent in FPGAs).

30. Referring to claim 15, Trimberger, as modified, has taught a computer processor according to claim 1, wherein at least one configurable operator of the second data execution path is capable of executing data processing instructions with an execution depth greater than two computations before returning results to a results store (Trimberger: column 3, lines 10-27) (It is inherent that these complex functions will take at least two cycles).

31. Referring to claim 16, Trimberger, as modified, has taught a computer processor according to claim 1, comprising a switch mechanism for receiving said operands from a

configurable data processing instruction and switching them as appropriate for supply to one or more of said configurable operators (Jacob, section 4.2 and Fig.2).

32. Referring to claim 17, Trimberger, as modified, has taught a computer processor according to claim 1, comprising a switch mechanism for receiving results from one or more of said configurable operators and switching the results as appropriate for supply to one or more of a result store and feed back loop (Trimberger: column 8, lines 51-59).

33. Referring to claim 18, Trimberger, as modified, has taught a computer processor according to claim 1, comprising a plurality of control maps for mapping configuration bits received from configurable data processing instructions to configuration information for supply to configurable operators of the second data execution path (See Jacob, Table 1 and Fig.2. Note that, in response to at least one FPGA function field bit, a control map (Reconfiguration Bits Table shown in Table 1) provides configuration information to the configurable operators).

34. Referring to claim 19, Trimberger, as modified, has taught a computer processor according to claim 1, comprising a switch mechanism for receiving configuration information from a control map and switching it as appropriate for supply to configurable operators of the second data execution path (See Jacob, Table 1 and Fig.2. Note that, in response to at least one FPGA function field bit, a control map (Reconfiguration Bits Table shown in Table 1) provides configuration information to the configurable operators).

35. Referring to claim 20, Trimberger, as modified, has taught a computer processor according to claim 1, comprising configurable operators selected from one or more of: multiply accumulate operators; arithmetic operators; state operators; and cross-lane permuters (Trimberger: column 3, lines 10-27).

36. Referring to claim 21, Trimberger, as modified, has taught a computer processor according to claim 1, comprising operators and an instruction set capable of performing one or more operations selected from: Fast Fourier Transforms; Inverse Fast Fourier Transforms; Viterbi encoding/decoding; Turbo encoding/decoding; and Finite Impulse Response calculations; and any other Correlations or Convolutions (Trimberger: column 3, lines 10-27) (polynomial evaluation is used in FFT and IFFT).

37. Referring to claim 22, Trimberger has taught a method of operating a computer processor having control and data processing capabilities, said computer processor comprising:

a) a decode unit for decoding instructions (Fig.2, component 112).

b) a dedicated control processing facility comprising a control execution path dedicated to processing control instructions having its own control register file (Fig.2, component 103 or 140, for instance) and an execution unit (Fig.2, component 100). Note that at least these components may be combined and called a dedicated control processing facility.

c) a dedicated data processing facility (Fig.2, at least component 120) dedicated to processing data processing instructions, separate from said dedicated control processing facility, having its own data register file (Fig.2, at least 130) separate from said control register file, the data processing facility comprising a controller (controllers inherently exist in processors).

d) Trimberger has not taught that the data processing facility comprises a first data execution path including fixed operators and a second data execution path including at least configurable operators, both of said first and second data execution paths separate from said control execution path and each other, said configurable operators pre-configured into a plurality of hardwired operator classes. However, Haynes, Lodi, and Madurawe have taught that FPGAs may be

designed to include dedicated circuitry in addition to reconfigurable circuitry. Specifically, Haynes has taught dedicated multiplier blocks, which may be programmably interconnected to create larger multipliers. Similarly, Lodi has taught dedicated carry chains, which may be connected to form, among other things, absolute value and logic function circuitry. See page 133 and sections 3.3 and 4. Madurawe has taught dedicated adders and I/O circuitry in an FPGA for common operations. See column 6, lines 2-4. Essentially, instead of a fully reprogrammable FPGA, as taught by Trimberger, Haynes, Lodi, and Madurawe have taught programmable devices, such as FPGAs, that include fixed and configurable circuitry. Such a configuration, which is common in a Xilinx Virtex FPGA, for instance, allows programmers to achieve balance between programmability and speed for different applications. One of ordinary skill in the art would have recognized that the hardwired operators of Haynes, Lodi, and Madurawe could be implemented in the FPGA of Trimberger. Such a modification would allow Trimberger to achieve increased speed in cases where dedicated circuitry is faster than programmable circuitry. As a result, in order to increase speed for common operations, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify Trimberger's gate array such that the data processing facility (Trimberger, Fig.2, at least component 120) comprises a first data execution path including fixed operators (for instance, a fixed adder and I/O path, as taught by Madurawe) and a second data execution path including at least configurable operators (for instance, a configurable multiplier and carry-chain path, as taught by Haynes and Lodi), both of said first and second data execution paths separate from said control execution path and each other (clearly the FPGA paths are separate from each other and from the control path), said configurable operators pre-configured into a plurality of hardwired operator classes (in the

proposed combination, the FPGA of Trimberger, as modified, would include configurable operators pre-configured into hardwired multiplier and carry chain classes).

e) Trimberger has further taught that the method comprises separating, with said decode unit, control instructions from data processing instructions. See Fig.2, component 112 and column 7, lines 45-50. The examiner asserts that the decoder inherently operates as claimed as the whole purpose of a decoder is to determine the type of instruction and generate the appropriate control signals 113 to control the appropriate circuitry to perform the desired operation. Clearly, if the instruction is meant for execution unit 100, then an instruction for that unit will be determined and signals for that unit will be supplied by the decoder.

f) Trimberger has further taught supplying, by said decode unit, one of said control instructions to a functional unit in said dedicated control processing facility. See Fig.2. The decoder will send control instructions (any instruction that may be executed by the dedicated control processing facility) to the dedicated control processing facility.

g) Trimberger has further taught that the method comprises decoding a plurality of instructions to detect whether at least one of said data processing instructions of said plurality of instructions defines a fixed data processing instruction or a configurable data processing instruction. See Fig.2, component 112. This is again deemed inherent. If an instruction is a fixed path instruction, then appropriate signals will be sent to the fixed FPGA circuitry. If the instruction is a configurable instruction, then appropriate signals will be sent to the configurable FPGA circuitry.

h) Trimberger has further taught that the method comprises causing the computer processor to supply said at least one of said data processing instructions to said first data execution path for

processing when said fixed data processing instruction is detected and to said second data execution path for processing when said configurable data processing instruction is detected; and outputting results produced by said first data execution path when a fixed data processing instruction is detected and outputting results produced by said data execution path when a configurable processing instruction is detected. This is deemed inherent. Clearly, if the FPGA is to perform a particular add, then the fixed adder will be used to execute the add and produce a result. Similarly, if an absolute value is to be performed, the configurable carry-chain will be used to produce a result.

i) Trimberger has not taught that the dedicated control processing facility also includes functional units comprising a branch unit and a load/store unit. However, the examiner asserts that such units are very well known in the art and are advantageous for providing basic functionality. Branch units are clearly advantageous because they allow for execution of branch instructions. These are at least useful so that loops may be implemented. Loops allow for repeated execution of a block of code without writing the code repetitively within the program. Hence, code size may be decreased. Load and stores, on the other hand, allow for communication data to/from the register file and memory, thereby expanding the usable memory space. As a result, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify Trimberger such that the dedicated control processing facility includes a branch unit and load/store unit.

j) Trimberger has not taught that said configurable data processing instruction indicates at least one operand to be processed and includes an opcode portion defining the operation to be carried out on the operand, and configuring the connectivity of said configurable operators in accordance

with configuration information provided in said opcode portion of said configurable data processing instruction, wherein said configurable operators are arranged to receive said at least one operand. That is, Trimberger is fairly silent on how the FPGA is reconfigured. However, Jacob has taught than an FPGA instruction including an opcode and operands is one way to reconfigure an FPGA. See section 4.2 and Fig.2. Note the FPGA reconfiguration instruction has an opcode (Fig.2 and Table 1, "FPGA function" field) that defines the operation, and at least one operand to be processed (Fig.2, "Rsource" field). One of ordinary skill in the art would have recognized how straightforward configuration and operation using this configuration on operands would be using such an instruction. In addition, this instruction allows for the configuration and the operation to be triggered with just a single instruction. This is more efficient than an instruction to configure followed by an instruction to trigger operation using that configuration. When a configuration instruction is decoded and detected, it specifies the configuration the FPGA should take on and also the data that is to be processed by the configuration. As a result, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify Trimberger to include a special said configurable data processing instruction that indicates at least one operand to be processed and includes an opcode portion defining the operation to be carried out on the operand, and configuring the connectivity of said configurable operators in accordance with configuration information provided in said opcode portion of said configurable data processing instruction, wherein said configurable operators are arranged to receive said at least one operand. This is a simple and straightforward way to program the FPGA in Trimberger.

38. Referring to claim 30, Trimberger has taught a hardware computer processor having control and data processing capabilities comprising:

a) a hardware decode unit for decoding instructions and operable to separate control instructions from data processing instructions (Trimberger: Figure 2, item 112). Control instructions for execution unit 100 and data processing instructions for FPGA 120 are inherently separated because the purpose of the decoder is to identify the type of instruction and control the appropriate circuitry to carry out the operation indicated by the instruction. Therefore, if a control instruction exists, appropriate control signals would be sent to unit 100. If a data processing instruction exists, appropriate control signals would be sent to FPGA 120.

b) a dedicated hardware control processing facility comprising a control execution path dedicated to processing said control instructions having its own control register file (Fig.2, component 103 or 140, for instance) and a hardware execution unit (Fig.2, component 100). Note that at least these components may be combined and called a dedicated control processing facility.

c) a dedicated hardware data processing facility (Fig.2, at least component 120) dedicated to processing said data processing instructions, separate from said dedicated control processing facility, having its own data register file (Fig.2, at least component 130) separate from said control register file, the data processing facility comprising a controller (controllers inherently exist in processors).

d) Trimberger has not taught that the data processing facility comprises a first data execution path including fixed operators and a second data execution path including at least configurable operators, both of said first and second data execution paths separate from said control execution path and each other, said configurable operators pre-configured into a plurality of hardwired

operator classes. However, Haynes, Lodi, and Madurawe have taught that FPGAs may be designed to include dedicated circuitry in addition to reconfigurable circuitry. Specifically, Haynes has taught dedicated multiplier blocks, which may be programmably interconnected to create larger multipliers. Similarly, Lodi has taught dedicated carry chains, which may be connected to form, among other things, absolute value and logic function circuitry. See page 133 and sections 3.3 and 4. Madurawe has taught dedicated adders and I/O circuitry in an FPGA for common operations. See column 6, lines 2-4. Essentially, instead of a fully reprogrammable FPGA, as taught by Trimberger, Haynes, Lodi, and Madurawe have taught programmable devices, such as FPGAs, that include fixed and configurable circuitry. Such a configuration, which is common in a Xilinx Virtex FPGA, for instance, allows programmers to achieve balance between programmability and speed for different applications. One of ordinary skill in the art would have recognized that the hardwired operators of Haynes, Lodi, and Madurawe could be implemented in the FPGA of Trimberger. Such a modification would allow Trimberger to achieve increased speed in cases where dedicated circuitry is faster than programmable circuitry. As a result, in order to increase speed for common operations, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify Trimberger's gate array such that the data processing facility (Trimberger, Fig.2, at least component 120) comprises a first data execution path including fixed operators (for instance, a fixed adder and I/O path, as taught by Madurawe) and a second data execution path including at least configurable operators (for instance, a configurable multiplier and carry-chain path, as taught by Haynes and Lodi), both of said first and second data execution paths separate from said control execution path and each other (clearly the FPGA paths are separate from each other and from the control path), said

configurable operators pre-configured into a plurality of hardwired operator classes (in the proposed combination, the FPGA of Trimberger, as modified, would include configurable operators pre-configured into hardwired multiplier and carry chain classes).

d) Trimberger has further taught a switch mechanism for receiving data processing operands from a configurable data processing instruction and switching them as appropriate for supply to one or more of said configurable operators. See, Trimberger, column 7, lines 45-50. When an instruction calls for an operation using the configurable operators, then operands will be supplied to them. For instance, as described above, multipliers may be one group of configurable operators. To perform multiplication, multiple input values (operands) are needed. These operands are therefore switched to the operators for execution.

e) Trimberger has further taught that said decode unit is operable to supply a said control instruction to a functional unit in said dedicated control processing facility and operable to detect whether one of said data processing instructions defines a fixed data processing instruction or a configurable data processing instruction, said decode unit causing the computer processor to supply said one of said data processing instructions to said first data execution path for processing when a fixed data processing instruction is detected and to said second data execution path for processing when a configurable data processing instruction is detected. See Fig.2, component 112 and column 7, lines 45-50. The examiner asserts that decoders inherently operation in the claimed fashion. They distinguish all types of instructions from each other, and produce the appropriate control signals 113 to control the appropriate circuitry to perform the desired operation.

f) Trimberger has not taught that the dedicated control processing facility also includes functional units comprising a branch unit (despite hinting at existence of a branch unit with disclosure of condition codes (Fig.2)) and a load/store unit. However, the examiner asserts that such units are very well known in the art and are advantageous for providing basic functionality. Branch units are clearly advantageous because they allow for execution of branch instructions. These are at least useful so that loops may be implemented. Loops allow for repeated execution of a block of code without writing the code repetitively within the program. Hence, code size may be decreased. Load and stores, on the other hand, allow for communication data to/from the register file and memory, thereby expanding the usable memory space. As a result, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify Trimberger such that the dedicated control processing facility includes a branch unit and load/store unit.

g) Trimberger has not taught that said configurable data processing instruction indicates at least one operand to be processed and includes an opcode portion defining the operation to be carried out on the operand, and that said configurable operators are arranged to receive said at least one operand, and that said controller is operable to configure the connectivity of said configurable operators in accordance with configuration information provided in the opcode portion of said configurable data processing instruction. That is, Trimberger is fairly silent on how the FPGA is reconfigured. However, Jacob has taught than an FPGA instruction including an opcode and operands is one way to reconfigure an FPGA. See section 4.2 and Fig.2. Note the FPGA reconfiguration instruction has an opcode (Fig.2 and Table 1, “FPGA function” field) that defines the operation, and at least one operand to be processed (Fig.2, "Rsource" field). One of

ordinary skill in the art would have recognized how straightforward configuration and operation using this configuration on operands would be using such an instruction. In addition, this instruction allows for the configuration and the operation to be triggered with just a single instruction. This is more efficient than an instruction to configure followed by an instruction to trigger operation using that configuration. When a configuration instruction is decoded and detected, it specifies the configuration the FPGA should take on and also the data that is to be processed by the configuration. As a result, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify Trimberger to include a special configurable data processing instruction that indicates at least one operand to be processed and includes an opcode portion defining the operation to be carried out on the operand, and that said configurable operators are arranged to receive said at least one operand, and that said controller is operable to configure the connectivity of said configurable operators in accordance with configuration information provided in the opcode portion of said configurable data processing instruction. This is a simple and straightforward way to program the FPGA in Trimberger.

39. Referring to claim 31, claim 31 is rejected for the same reason set forth in the rejection of claim 5.

40. Referring to claim 32, claim 32 is rejected for the same reason set forth in the rejection of claim 12.

Response to Arguments

41. Applicant's arguments have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

42. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Applicant is reminded that in amending in response to a rejection of claims, the patentable novelty must be clearly shown in view of the state of the art disclosed by the references cited and the objections made. Applicant must also show how the amendments avoid such references and objections. See 37 CFR § 1.111(c).

Palem et al., U.S. Patent Application Publication No. US 2002/0174266 A1, has taught an API for reconfigurable computing systems. The API includes configure instructions, which specify the configuration, and write instructions, which specify operands and the configuration to be used to operate on the operands. See Fig.5.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to DAVID J. HUISMAN whose telephone number is (571)272-4168. The examiner can normally be reached on Monday-Friday (8:00-4:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/David J. Huisman/
Primary Examiner, Art Unit 2183